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Roger Fulghum
Baker & Butts, L.L.P.
One Shell Plaza
910 Louisiana
Houston, TX 77002-4995

EXAMINER	
KING, JUSTIN	
ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/768,665	Applicant(s) NGUYEN ET AL.	
	Examiner Justin I. King	Art Unit 2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 January 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 January 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Specification

1. The abstract of the disclosure is objected to because it exceeds the maximum of 150 words. Correction is required. See MPEP § 608.01(b).

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: "System and method for handling software system management interrupts in a multiprocessor computer system".

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the claims 17-18, 23, and 27's dedicated CPU for processing interrupt must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1-27 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitation "a first processor" in line 6. There is sufficient antecedent basis for this limitation in the claim. Claim 1 recites the limitation "the register contents" in line 11, "the system management interrupt handler" in lines 13 and 16, "the contents" in lines 14 and 16, "the memory" in line 14, and "the handling" in line 17. There are insufficient antecedent bases for these limitations in the claim. Examiner recommends removing the "the" or changing the "the" to "a". Claims 2-8 are rejected because they incorporate claim 1's limitations.

Claim 2 recites the limitation "a multiprocessor computer system" in lines 20-21 and "a second processor" in line 22. There are sufficient antecedent bases for these limitations in the claim. Examiner recommends changing the "a" to "the".

Claim 3 recites the limitation "a multiprocessor computer system" in lines 25-26 and "the responsibility" in lines 26-27. There are sufficient and insufficient antecedent bases for these limitations in the claim. Examiner recommends removing the "the" and changing the "a" to "the".

Claim 4 recites the limitation "a multiprocessor computer system" in lines 2-3 and "the same processor" in line 3. There are sufficient and insufficient antecedent bases for these limitations in the claim.

Claim 5 recites the limitation "a multiprocessor computer system" in lines 5-6 and "a first processor" in line 6, and "a command" in line 6, and "a software application" in lines 6-7, and "a system management interrupt" in line 7, and "the chip set" in line 8. There are sufficient and

insufficient antecedent bases for these limitations in the claim. Furthermore, claim 5 also recites "the processor" in line 8, it is unclear which processor this is referring to.

Claim 6 recites the limitation "a multiprocessor computer system" in lines 11-12, and "the PCI bridge" in line 12. There are sufficient and insufficient antecedent bases for these limitations in the claim.

Claim 7 recites the limitation "a multiprocessor computer system" in lines 15-16 and "the expansion bridge" in lines 16-17. There are sufficient and insufficient antecedent bases for these limitations in the claim.

Claim 8 recites the limitation "a multiprocessor computer system" in lines 19-20 and "an instruction" in lines 20-21. There are sufficient and insufficient antecedent bases for these limitations in the claim.

Claim 9 recites the limitation "the storage" in line 7, "the contents" in line 7, "the register" in line 7, and "a processor" in line 8, and "the issuance" in line 9, and "the case" in line 11, and "the software system management interrupt" in lines 12-13, and "the parameter" in line 13, and "the instruction" in line 14. There are sufficient and insufficient antecedent bases for these limitations in the claim. Examiner recommends removing the "the" or changing the "the" to "a". Furthermore, claim 9 recites "the processor" in lines 11, 12, and 13-14; the claim language is unclear on whether it is referring to the first processor or the second processor. Claims 10-15 are rejected because they incorporate claim 9's limitations.

Claim 10 recites "the processor" in line 16; the claim language is unclear on whether it is referring to the first processor or the second processor.

Claim 12 recites the limitation "the PCI bridge" in lines 24-25. There is insufficient antecedent basis for this limitation in the claim.

Claim 13 recites the limitation "the expansion bus bridge" in lines 1-2. There is insufficient antecedent basis for this limitation in the claim.

Claim 14 recites the limitation "the issuance" in line 5. There is insufficient antecedent basis for this limitation in the claim. Furthermore, claim 14 recites "the processor" in line 5; it is unclear on whether it is referring to the first processor or the second processor.

Claim 15 recites the limitation "the issuance" in line 10. There is insufficient antecedent basis for this limitation in the claim. Furthermore, claim 15 recites "the processor" twice in line 9; it is unclear on whether it is referring to the first processor or the second processor.

Claim 16 recites the limitation "the processor" in line 2, "the handling" in lines 2-3, "the content" and "the register content" in line 11, "the receipt" in line 16. There are insufficient antecedent bases for these limitations in the claim. Furthermore, claim 16 recites "the processor" in lines 5 and 9; it is unclear on whether it is referring to the first processor (line 4) or not. Claims 17-21 are rejected because they incorporate claim 16's limitations.

Claim 17 recites the limitation "a multiprocessor computer system" in lines 22-23 and "a system management interrupt handler" in line 23. There are sufficient antecedent bases for these limitations in the claim.

Claim 18 recites the limitation "a multiprocessor computer system" in lines 25-26 and "a system management interrupt handler" in line 26. There are sufficient antecedent bases for these limitations in the claim.

Claim 19 recites the limitation "a multiprocessor computer system" in lines 1-2. There is a sufficient antecedent basis for this limitation in the claim.

Claim 20 recites the limitation "a multiprocessor computer system" in lines 5-6 and "the PCI bridge" in line 7. There are sufficient and insufficient antecedent bases for these limitations in the claim.

Claim 21 recites the limitation "a multiprocessor computer system" in lines 9-10 and "the expansion bus bridge" in line 11. There are sufficient and insufficient antecedent bases for these limitations in the claim.

Claim 22 recites the limitation "the saved context" in lines 4, 6, 8, "the instruction" in line 7, "the parameters" in line 8, and "the handling" in lines 8-9. There are insufficient antecedent bases for these limitations in the claim. Claims 23-27 are rejected because they incorporate claim 22's limitations.

Claim 23 recites the limitation "a multiprocessor computer system" in line 11 and "the same" in line 12. There are sufficient and insufficient antecedent bases for these limitations in the claim.

Claim 24 recites the limitation "a multiprocessor computer system" in line 15, "the instruction" in line 16, and "the chip set" in line 17. There are sufficient and insufficient antecedent bases for these limitations in the claim.

Claim 25 recites the limitation "a multiprocessor computer system" in line 19, and "the PCI bridge" in line 20. There are sufficient and insufficient antecedent bases for these limitations in the claim.

Claim 26 recites the limitation "a multiprocessor computer system" in line 23, and "the expansion bus bridge" in line 24. There are sufficient and insufficient antecedent bases for these limitations in the claim.

Claim 27 recites the limitation "a multiprocessor computer system" in line 1 and "the handling" in line 6. There are sufficient and insufficient antecedent bases for these limitations in the claim.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

7. Claims 1, 5-16, and 19-22 are rejected under 35 U.S.C. 102(a) as being anticipated by Tyner et al. (U.S. Patent No. 6,272,618) or Goodman et al. (U.S. Patent No. 6,282,601).

Referring to claim 1: Tyner discloses a method for handling system management interrupts in a multiprocessor computer system, comprising the steps of: writing a predetermined signature to a predetermined register of the first processor (the program counter disclosed in column 4, lines 41-42); executing in a first processor a command of a software application to cause the first processor to initiate a system management interrupt (column 3, line 37); receiving at each processor an instruction that a software system management interrupt has been issued (figure 2, steps 102-106); entering system management mode at each processor (figure 2, step 104); saving the register contents of each processor to a memory space associated with each

respective processor (figure 2, step 106); selecting a second processor as the system management interrupt handler (figure 2, step 120); scanning the contents of the memory space associated with each processor (column 4, lines 40-42); and when the second processor locates the saved predetermined signature in one of the memory spaces associated with the processors of the computers system, using the contents of the memory space associated with the predetermined signature for any parameters necessary for the handling of the system management interrupt (figure 3,steps 130, 132). Hence, claim 1 is anticipated by Tyner.

Goodman discloses a method for handling system management interrupts in a multiprocessor computer system, comprising the steps of: writing a predetermined signature (the identifying signature disclosed in column 2, line 15, and figure 3, step 104) to a predetermined register of the first processor; executing in a first processor a command of a software application to cause the first processor to initiate a system management interrupt (column 1, line 29); receiving at each processor an instruction that a software system management interrupt has been issued (figure 3, step 106); entering system management mode at each processor; saving the register contents of each processor to a memory space associated with each respective processor (figure 3, step 106); selecting a second processor as the system management interrupt handler (column 1, lines 46-49); scanning the contents of the memory space associated with each processor (figure 4, steps 126, 128, and 130); and when the second processor locates the saved predetermined signature in one of the memory spaces associated with the processors of the computers system, using the contents of the memory space associated with the predetermined signature for any parameters necessary for the handling of the system management interrupt (figure 4, steps 134, 136, and 138). Hence, claim 1 is anticipated by the Goodman.

Referring to claim 5: Claim 1's argument applies; Tyner discloses that the processor writes to the memory (figure 1, structure 18) via the chip set's port (figure 1, structure 16). Goodman discloses that the processor writes to the memory (figure 1, structure 26) via the chip set's port (figure 1, structure 18). Furthermore, Applicant also discloses the processors' access to chip set's I/O port as one standard well-known system activities (Application, page 3, lines 8-9).

Referring to claim 6: Claim 5's argument applies; furthermore, both Tyner and Goodman's chip sets are a PCI bridge.

Referring to claim 7: Claim 5's argument applies; furthermore, Tyner discloses an expansion bridge (figure 1, structure 42) and Goodman discloses an expansion bridge (figure 1, structure 50).

Referring to claim 8: Claim 7's argument applies; furthermore, Tyner discloses that each of the processors of the system to enter system management mode (column 4, lines 9-10), and Goodman also discloses that each of the processors of the system to enter system management mode (column 1, lines 50-54).

Referring to claim 9: Tyner discloses a computer system, comprising a first processor (figure 1, structure 12a); a second processor (figure 1, structure 122b); a chip set (figure 1, structure 16) including a bus bridge coupling a first bus (figure 1, structure 15) of a first format to a second bus (figure 1, structure PCI bus) of a second format; a memory having a memory space reserved for each processor of the computer system (column 2, lines 64-66), the reserved memory space being used for the storage of the contents of the register of each processor in the event that a processor of the computer system enters system management mode; and wherein

each of the processors is capable of issuing an instruction causing the issuance of a system management interrupt (figure 2, step 100, column 3,lines 36) and thereby causing each of the processors to receive from the chip set a system management interrupt (column 4, lines 9-10), and, in the case of the processor selected for the handling of the interrupt, scanning the memory space to locate a signature (figure 3, steps 120 and 122) issued by the processor initiating the software system management interrupt to permit the selected processor to locate the parameters passed by the processor that issued the instruction that caused the issuance of the system management interrupt. Hence, claim 9 is anticipated by Tyner.

Goodman discloses a computer system, comprising a first processor (figure 1, structure 12a); a second processor (figure 1, structure 12b); a chip set (figure 1, structure 18) including a bus bridge coupling a first bus (figure 1, structure 14) of a first format to a second bus (figure 1, structure 20) of a second format; a memory having a memory space reserved for each processor of the computer system (figure 2), the reserved memory space being used for the storage of the contents of the register of each processor in the event that a processor of the computer system enters system management mode; and wherein each of the processors is capable of issuing an instruction causing the issuance of a system management interrupt and thereby causing each of the processors to receive from the chip set a system management interrupt (figures 3-4, column 1, lines 50-54), and, in the case of the processor selected for the handling of the interrupt, scanning the memory space to locate a signature (steps 124 and 126) issued by the processor initiating the software system management interrupt to permit the selected processor to locate the parameters passed by the processor that issued the instruction that caused the issuance of the system management interrupt. Hence, claim 9 is anticipated by Goodman.

Referring to claim 10: Claim 9's argument applies; furthermore, Tyner discloses the write instruction (column 2, lines 25-26); Goodman also discloses the write instruction (claim 10). Furthermore, the write operation is a standard system I/O operation.

Referring to claim 11: Both Tyner and Goodman disclose that the write instruction is received by the chip set of the computer system; and wherein the chip set of the computer system issues the instruction that causes the processors of the system to enter system management mode (Tyner's column 1, lines 48-54; Goodman's column 1, lines 30-45). \

Referring to claim 12: Claim 11's argument applies; furthermore, claim 12 is rejected over the claim 6's argument.

Referring to claim 13: Claim 11's argument applies; furthermore, claim 13 is rejected over the claim 7's argument.

Referring to claims 14-15: Claim 9's argument applies; furthermore, both Tyner and Goodman disclose that each processor includes a predetermined register for receiving a data signature indicating that the processor of the register caused the issuance of a software system management interrupt (Tyner's program counter disclosed in column 4, lines 41-42; Goodman's identifying signature disclosed in column 2, line 15, and figure 3, step 104).

Referring to claim 16: Tyner disclose a method for handling system management interrupts in a multiprocessor computer system comprising the steps of issuing an instruction (figure 2, step 100) from a first processor of the system to a chip set of the computer system; receiving the instruction at the chip set of the computer system and, in response, issuing a command causing the processors of the system to enter system management mode (figure 2, steps 104 and 106); writing a software system management interrupt signature (the program

counter disclosed in column 4, lines 41-42) to a predetermined register of the first processor as an indication that the first processor issued the command that caused the processors of the system to enter system management mode; writing the content of the registers of each processor to a memory location (figure 2, step 106), the memory location including a memory space reserved for and associated with the register contents of each processor (column 2, lines 64-67); transmitting a software system management interrupt to a second processor of the computer system, the second processor including a system management interrupt handler, and the second processor locating, in response, to the receipt of the software system management interrupt the software system management interrupt signature in the memory location; and retrieving (figure 3, steps 120 and 122) for use by the system management interrupt handler as parameters register contents saved by the first processor to the memory space associated with the software system management interrupt. Hence, claim 16 is anticipated by Tyner.

Goodman discloses a method for handling system management interrupts in a multiprocessor computer system comprising the steps of issuing an instruction (software interrupt disclosed in column 1, line 29) from a first processor of the system to a chip set of the computer system; receiving the instruction at the chip set of the computer system and, in response, issuing a command causing the processors of the system to enter system management mode; writing a software system management interrupt signature to a predetermined register of the first processor as an indication that the first processor (figure 3, step 104) issued the command that caused the processors of the system to enter system management mode (column 1, lines 50-54); writing the content of the registers of each processor to a memory location, the memory location including a memory space reserved for and associated with the register

contents of each processor; transmitting a software system management interrupt to a second processor of the computer system (figure 4, step 126), the second processor including a system management interrupt handler, and the second processor locating, in response, to the receipt of the software system management interrupt the software system management interrupt signature in the memory location; and retrieving (figure 4, step 126) for use by the system management interrupt handler as parameters register contents saved by the first processor to the memory space associated with the software system management interrupt. Hence, claim 16 is anticipated by Goodman.

Referring to claim 19: Claim 16's argument applies; furthermore, claim 19 is rejected over the claim 5's argument.

Referring to claim 20: Claim 19's argument applies; furthermore, claim 20 is rejected over the claim 6's argument.

Referring to claim 21: Claim 19's argument applies; furthermore, claim 21 is rejected over the claim 7's argument.

Referring to claim 22: Tyner discloses a method for handling system management interrupt in a multiprocessor computer system comprising the steps of receiving at one of the processors of the computer system a system management interrupt (figure 2, steps 102-106); scanning (column 4, lines 40-42) the memory location containing the saved context of each processor of the computer system; locating in the memory location a signature identifying the saved context of the processor that issued the instruction that caused the system management interrupt; and retrieving from the saved context of the processor the parameters necessary for the

handling of the system management interrupt (figure 3, steps 130 and 132). Hence, claim 22 is anticipated by Tyner.

Goodman discloses a method for handling system management interrupt in a multiprocessor computer system comprising the steps of receiving at one of the processors of the computer system a system management interrupt (column 1, lines 47-49); scanning the memory location containing the saved context of each processor of the computer system (figure 4, steps 126, 128, and 130); locating in the memory location a signature identifying the saved context of the processor that issued the instruction that caused the system management interrupt; and retrieving from the saved context of the processor the parameters necessary for the handling of the system management interrupt (figure 4, step 134). Hence, claim 22 is anticipated by Goodman.

8. Claims 2 are rejected under 35 U.S.C. 102(a) as being anticipated by Goodman.

Referring to claim 2: Claim 1's argument applies; furthermore, Goodman discloses an arbitration scheme (the interrupt controller disclosed in column 1, line 46-47).

9. Claims 4 are rejected under 35 U.S.C. 102(a) as being anticipated by Tyner.

Referring to claim 4: Claim 1's argument applies; furthermore, Tyner discloses locating the processor, which causes the interrupt (column 4, lines 33-34, figure 3, step 120).

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

12. Claims 3, 17-18, and 23-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of the Goodman and the Operating System Concepts (OSC) by James L. Peterson and Abraham Silberschatz.

Referring to claim 3: Claim 2's argument applies, but Goodman does not explicitly disclose assigning interrupt to each processor in turn. The OSC, as a popular academic textbook, discloses the round robin scheme for allocating processing resources / workload in turn. Therefore, it would have been obvious to one having ordinary skill in the computer art to adapt OSC's teaching to Goodman because OSC teaches one to sequential processing the system tasks to equally distribute the workloads.

Referring to claims 17-18, 23, and 27: Goodman does not explicitly disclose dedicated interrupt processing CPU. Although prior art does not disclose dedicated interrupt CPU, such

limitation is merely a matter of design choice and would have been obvious. The prior art teaches signature associated with each processor and interrupt. The limitations of dedicated CPU does not define a patentably distinct invention over that in prior arts since both the invention as a whole and combined prior arts are directed to locate the interrupt initiating CPU's saved data. The limitation of dedicated interrupt processing CPU is inconsequential for the invention as a whole and presents no new or unexpected results, so long as the saved data is retrieved. Therefore, to have the dedicated CPU as claimed would have been a matter of obvious design choice to one of ordinary skill in the computer art.

Referring to claim 24: Claim 23's argument applies; furthermore, claim 24 is rejected over the claim 5's argument.

Referring to claim 25: Claim 24's argument applies; furthermore, claim 25 is rejected over the claim 6's argument.

Referring to claim 26: Claim 25's argument applies; furthermore, claim 26 is rejected over the claim 7's argument.

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Justin King whose telephone number is (703) 305-4571. The examiner can normally be reached on Monday through Friday from 9:00 A.M. to 5:00 P.M..

If attempts to reach the examiner by telephones are unsuccessfully, the examiner's supervisor, Mark Reinhart can be reached at (703) 308-3110.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose number is (703)-306-5631.

Justin King
July 29, 2003

Gopal C. Ray

GOPAL C. RAY
PRIMARY EXAMINER
GROUP 2180